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Chapter 1: Device Physics

1.1. Aluminum and gallium are group-III elements; arsenic is a group-V element. Each atom of a group-III element adds one hole to the semiconductor, while each atom of a group-V element adds one electron. In order for the semiconductor to be intrinsic, the number of holes added must equal the number of electrons added. The sum of the numbers of aluminum and gallium atoms must therefore equal the number of phosphorus atoms. Expressed as a chemical formula, intrinsic aluminum gallium arsenide is $Al_xGa_{1-x}As$, where $0 < x < 1$.

1.2. Silicon doped with 10^{16} atoms/cm^3 of boron and 10^{16} atoms/cm^3 of phosphorus would contain exactly equal numbers of holes and electrons generated by the ionization of the dopants. These carriers would recombine, leaving only a small number of thermally generated carriers. The silicon would thus act as if it were intrinsic. In practice, it is impossible to meter the dopants with sufficient precision to achieve a residual carrier concentration as low as intrinsic silicon (about 10^{10} electrons/cm^3 and 10^{10} holes/cm^3 at 25°C). Instead, the silicon will either be very lightly doped N-type or very lightly doped P-type, depending upon which dopant is present in excess.

1.3. Boron is a group-III element and phosphorus is a group-V element. A concentration of $5 \cdot 10^{16}$ atoms/cm^3 of boron would thus generate $5 \cdot 10^{16}$ holes/cm^3. A concentration of $8 \cdot 10^{16}$ atoms/cm^3 of phosphorus would generate $8 \cdot 10^{16}$ electrons/cm^3. The $5 \cdot 10^{16}$ holes/cm^3 would recombine with a like quantity of electrons, leaving $3 \cdot 10^{16}$ electrons/cm^3 remaining.

1.4. Diamond is the cubic modification of carbon. Like silicon, it is an elemental semiconductor. Boron is a group-III element and therefore each atom of boron introduced into the diamond generates a hole. These holes are responsible for the conductivity of blue diamonds. Natural boron-doped blue diamonds are called *type IIb-diamonds*.[1]

1.5. The leakage current flowing through a reverse-biased PN diode doubles approximately every eight degrees Celsius. Given two temperatures T_1 and T_2, the corresponding leakage currents I_1 and I_2 will satisfy the equation

$$I_2 = I_1 \cdot 2^{(T_2 - T_1)/8°C}$$

Given that T_1 = 25°C, I_1 = 1 pA, and T_2 = 125°C, the above equation gives I_2 = 5.8 nA. Similarly, at T_2 = 175°C, it gives 440 nA. The leakage at 125°C is sufficient to upset sensitive low-current analog circuitry, while the leakage at 175°C is enough to upset many, if not most, analog circuits. Thus, while this diode could probably be used in many circuits at 125°C, its usefulness would be limited at 175°C.

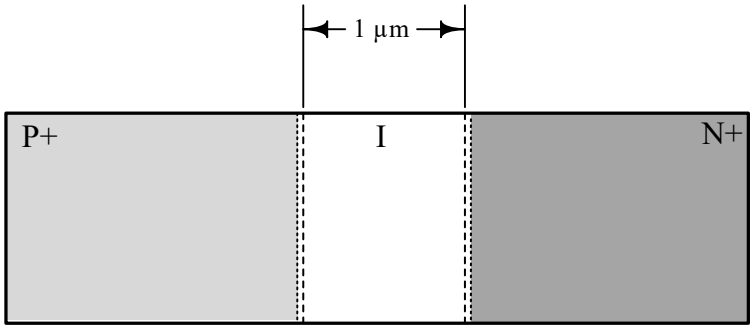


Figure 1.6. Sketch of PIN structure for Exercise 1.6.

[1] J. M. King, T. M. Moses, J. E. Shigley, C. M. Welbourn, S. C. Lawson, and M. Cooper, "Characterizing natural-color Type IIB blue diamonds," *Gems and Gemology*, Winter 1998, pp. 246–268.

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1.6. The layer of intrinsic silicon is denoted "I" in Figure 1.6. The dashed lines mark the metallurgical junctions between P+ and intrinsic silicon, and between N+ and intrinsic silicon. The dotted lines bounding the shaded regions mark the limits of the depletion region, which extends entirely through the intrinsic region and slightly into both the P+ and N+ silicon. The depletion region must uncover equal numbers of acceptors in the P+ silicon and donors in the N+ silicon. These charges sweep carriers out of the depletion region and support the built-in potential across the structure. Since the intrinsic silicon contains neither acceptors nor donors, it does not contribute to the charges within the depletion region. This type of structure is sometimes called a PIN diode. It finds use where a very wide depletion region is desired. The so-called intrinsic region is not in practice truly intrinsic because is not feasible to manufacture perfectly intrinsic silicon, but the very small space charge in this region represents only a negligible contribution to the overall charge balance.

1.7. Since cadmium sulfide is a semiconductor, impinging light of sufficiently short wavelengths will generate electrons and holes. If a voltage is placed across the photocell, the electrons will move towards the positive end of the device and the holes will move towards the negative end. These carriers constitute a current flow that is proportional to the intensity of the light striking the photocell. It is perhaps of interest to note that cadmium sulfide is a II-VI semiconductor. Dmitri Mendeleev assigned Roman numerals to the groups based upon a chemical property called valence, which for our purposes can be considered the number of electrons in the valence shell of the atom. Cadmium sulfide consists of equal numbers of cadmium and sulfur atoms and therefore has an average of four valence electrons per atom. The resulting material behaves as a semiconductor with a bandgap of about 2.4 eV.[2]

1.8. Normally, breakdown occurs near the surface of the junction between the N+ region and the P– region because the doping concentration in the P– region is highest here. One would therefore expect the depletion region to be narrowest here. This would correspond to the lowest breakdown voltage, and breakdown occurs preferentially at the point where the breakdown voltage is lowest. So far, the breakdown voltage appears to be set by the P– doping and not the N+ doping because the depletion region width is almost entirely controlled by the lighter-doped side of the junction. However, sidewall curvature must also be considered. A shallow N+ region would have a sharper sidewall curvature than a deeper N+ region. Sharply curved regions intensify the electric field and therefore reduce the breakdown voltage. This therefore suggests that the 10 V diode has the deeper N+ region.

1.9. The exercise does not state the precise construction of the transistor. Let us consider an idealized one-dimensional NPN transistor consisting of an N+ emitter, a P-type base, and an N– collector. This device is normally operated in the forward active region in which most of the collector voltage drops across the collector-base junction. The depletion region around this junction extends deep into the lightly doped collector. The wide depletion region enables the transistor to support a large collector-base voltage without breakdown. Swapping the emitter and collector terminals creates a device with an N– emitter and an N+ collector. The collector-base depletion region now extends primarily into the moderately doped base rather than the heavily doped collector. The depletion region will be narrower and the avalanche breakdown voltage will be correspondingly lower. It is possible that the device may be unable to reach this full avalanche voltage before the neutral base is entirely depleted and the transistor suffers punchthrough. Either way, the device will only be able to sustain a fraction of the collector-base voltage drop that it was formerly able to achieve. For a typical 40 V standard bipolar vertical NPN, the collector-base breakdown voltage V_{CBO} will equal about 60 V in the customary orientation where the emitter is heavily doped and the collector is lightly doped, whereas it will equal about 7 V in the opposite orientation.

[2] U. Pal, R. Silva-González, G. Martínez-Montes, M. Gracia-Jiménez, M. A. Vidal, and Sh. Torres, "Optical characterization of vacuum evaporated cadmium sulfide films," *Thin Solid Films,* Vol. 305, 1997, pp. 345–350.

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1.10. The heavy emitter doping of the two transistors suggests that they should have emitter injection efficiencies approaching unity. As long as the devices operate at moderate current levels to avoid low-current and high-current beta rolloff, their respective betas should depend almost entirely upon their respective Gummel numbers. The Gummel number for any specific conduction path across the quasineutral base equals the line integral of the effective base doping concentration from the base side of the emitter-base depletion region to the base side of the collector-base depletion region. If the base doping is halved but the quasineutral base width is doubled, then the Gummel number remains the same. Therefore, we would expect that the two transistors have the same beta. The equality will not be exact because of such factors as a slight decrease in emitter injection efficiency in the device with the more heavily doped base region, and slight differences in recombination rates caused by differing levels of recombination centers in the two transistors due to differences in their processing. Also, the "base width" specified by the exercise might not be the width of the quasineutral base, but instead the distance between the base-emitter and base-collector metallurgical junctions. If this were the case, differences in depletion region penetration into the base would also introduce a small error. Still, we would expect that the second transistor with the wider and more lightly doped base would have a beta very near that of the first transistor, or 60.

1.11. Contacts to silicon are generally Schottky barriers. Those to P-type silicon generally have considerably lower contact potentials than those to N-type silicon, but the barrier hinders current flow to both lightly doped P-type and N-type silicon. Increasing the doping reduces the depletion region width beneath the Schottky barrier, and once this is decreased sufficiently, direct electron tunneling can occur. This mechanism effectively shorts out the rectifying junction and creates an Ohmic junction. The more heavily doped the silicon, the narrower the depletion region and the easier it is for carriers to tunnel across. This manifests itself as a reduction in contact resistance at higher doping concentrations. Thus, the process engineer's suggestion is a reasonable one, but there is a potential problem: the base doping affects several other parameters of importance to designers. The obvious example is the sheet resistance of base resistors. More subtly, if the increased doping penetrates sufficiently far into the silicon, it will increase the base doping beneath the emitter of the vertical NPN transistor and thus reduce its beta. Keeping the increase in doping concentration to a very shallow region of the base immediately beneath the surface of the silicon would prevent a reduction in NPN gain and would minimize the shift in base sheet resistance.

1.12. This is something of a trick question because there is not a single possible answer, but rather two. First consider the case where the transistor is an NMOS. If this is the case, the negative threshold voltage means that it is a depletion transistor. Adding a bit of boron to the P-type backgate would make it more difficult to invert the channel, thus increasing the threshold voltage (making it more positive or less negative). This is reported to be what happens, so it is possible that the device is a depletion NMOS. Now consider the case where the transistor is a PMOS. If this is the case, the negative threshold voltage means that it is an enhancement transistor. Adding a bit of boron to the N-type backgate would make it less heavily doped and thus easier to invert, so the magnitude of the threshold voltage should diminish, which is what happens. So the transistor could be an enhancement-mode PMOS. In summary, the device is either a depletion-mode NMOS or an enhancement-mode PMOS.

1.13. Doubling the dielectric thickness would weaken the electric field projected by the gate and thus make the transistor more difficult to invert. This means that the threshold voltage should decrease (become less positive or possibly even become negative).

1.14. An NMOS transistor with a threshold of 0.5 V is an enhancement device. Applying $V_{GS} = 2.0$ V to this transistor will cause a channel to form. Applying $V_{DS} = 4.0$ V will place the device in saturation because $V_{DS} > V_{GS} - V_t$. If V_{GS} is doubled to 4.0 V, the device will remain in saturation, but the current will greatly increase. We can use the Shichman-Hodges equation for saturation, $I_D = \frac{1}{2}k\,(V_{GS} - V_t)^2$, to determine that the current would increase by a factor of $[(4 - 0.5)/(2 - 0.5)]^2 = 5.4$. On the other

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hand, keeping V_{GS} at 2.0 V and doubling V_{DS} to 8.0 V would have only a small effect upon the drain current due to channel length modulation. Since the channel length modulation factor λ has not been given, the change in drain current cannot be computed, but it will almost certainly be much smaller than 540%.

1.15. The base-emitter voltage of a silicon PN-junction diode under moderate forward bias exhibits a temperature coefficient of about –2 mV/°C. Cooling the device from 25°C to –40°C would increase its forward voltage by about 130 mV, raising it from 620 mV to 750 mV. Heating the device from 25°C to 125°C would reduce its forward voltage by about 200 mV, dropping it from 620 mV to 420 mV.

1.16. Moving the gate and backgate further apart deepens the channel and therefore increases the drain current that can flow through the transistor. The exact amount by which the current increases will depend upon a number of factors: the gate-to-source voltage V_{GS}, the backgate-to-source voltage V_{BS}, the drain-to-source voltage V_{DS}, and whether the channel region is uniformly doped, and whether the dimension which doubles is the channel depth set by the edges of the gate-channel and backgate-channel depletion regions, or whether the dimension is the distance between the gate-channel and backgate-channel metallurgical junctions. Regardless of such considerations, the current will increase if the gate and backgate move apart. Also, this same movement will make the transistor more difficult to pinch off, and will therefore increase the magnitude of the pinchoff voltage.

1.17. Placing 30 V across a 1000 µm-long uniformly doped monocrystalline silicon resistor generates an electric field of 30 V/1000 µm = 30 mV/µm = 300 V/cm. As mentioned in Section 1.1.3 of the text, monocrystalline silicon obeys Ohm's law up to perhaps 5 kV/cm. Since the resistor operates well below this field intensity, it will obey Ohm's law quite precisely.

1.18. The capacitance of a reverse-biased PN junction is caused by the presence of a depletion region around the junction. Since no significant current flows across the depletion region, it can be treated as an insulator. The depleted silicon therefore forms the dielectric of a capacitor, and the undepleted silicon on either side of the junction forms the two electrodes of the capacitor. The larger the reverse bias placed across the junction, the wider the depletion region grows and the smaller the capacitance becomes. This capacitance is called the depletion capacitance.

1.19. To solve this problem, we must first realize that the emitter does not penetrate far enough into the base to significantly constrict current flow from B_2 to B_1. If this is the case, then the voltage V_{BB} will be applied uniformly down the base of the device. If $V_{B2} > V_{B1} + 10$ V, and the emitter is located about one-third of the way from B_1 to B_2, then the voltage in the base adjacent to the emitter must be about 3.3 V. In order for current to flow from emitter to base, V_{EB} must exceed 3.3 V by the amount necessary to forward-bias a PN junction. The problem does not give a temperature, so we can assume a temperature of 25°C and a forward bias of perhaps 0.6 V. This means that V_{EB} must approach 4 V before current begins to flow. When this current begins to flow, the device behaves in a very unusual fashion. Holes injected from the emitter into the base flow towards B_1 since this is the negative end of the base. These minority carrier holes are charge carriers, just as are the majority carrier electrons already present in the base. Both the holes and the electrons can carry current through the portion of the base between the emitter and B_1, so this portion of the base becomes lower resistance (or higher conductivity) than the rest. This causes the voltage in the base adjacent to the emitter to diminish, which causes more emitter current to become injected into the base. This type of positive feedback mechanism is called *snapback* and the emitter-base voltage needed to initiate it is called the *trigger voltage*. Unijunction transistors were historically used to make oscillator circuits. A capacitor was connected from base to emitter and a resistor or current source was used to charge this capacitor. When the capacitor reached the trigger voltage, it suddenly discharged. The cycle then repeated again and again. These so-called *relaxation oscillators* were used to make sawtooth voltage waveforms.

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